We claim:

1. A method of fabricating an MRAM array on a substrate, comprising:

(a) forming a first conductive layer comprised of a plurality of sectioned first lines on a substrate;

(b) forming an array of magnetic tunnel junctions (MTJs) on the first conductive layer; and

(c) forming a second conductive layer comprised of a plurality of parallel second lines on said MTJs wherein an MTJ is formed at each location where a second line crosses over a sectioned first line and wherein said second lines have thinner and thicker regions.

2. The method of claim **1** wherein the first conductive layer is comprised of sectioned first lines formed on a first insulation layer and within a second insulation layer that is on the first insulation layer.

3. The method of claim **2** wherein said MTJs are coplanar with a third insulation layer that is formed on said second insulation layer and first conductive layer.

4. The method of claim **1** wherein said second conductive layer is comprised of second lines which are bit lines.

5. The method of claim **4** wherein a thinner region of a bit line is formed above an MTJ and has a thickness of about 0.02 to 0.3 microns.

6. The method of claim **4** wherein a thicker region of a bit line is not formed above an MTJ and has a thickness of about 0.08 to 1.1 microns.

7. The method of claim **4** wherein a thinner region of a bit line is a lower metal layer comprised of a first diffusion barrier layer or adhesion layer and a conductive layer which is copper or gold formed on the first diffusion barrier layer or adhesion layer.

8. The method of claim **7** wherein a thicker region of a bit line is comprised of said lower metal layer, a second diffusion barrier layer on the lower metal layer, and an upper metal layer on the second diffusion barrier layer.

9. The method of claim **8** wherein said first and second diffusion barrier layers are comprised of Ta/TaN or Ti/TiN and said upper metal layer has the same composition as the conductive layer in the lower metal layer.

10. The method of claim **3** further comprised of forming a fourth insulation layer on the third insulation layer, forming a fifth insulation layer on the fourth insulation layer, and forming an array of parallel word lines above said MTJs in said fifth insulation layer wherein said word lines are perpendicular to said second lines which are bit lines.

11. A method for fabricating an MRAM array on an MRAM chip, comprising:

(a) forming a first conductive layer comprised of a plurality of sectioned first lines in a second insulation layer on a substrate that has an upper first insulation layer;

(b) forming an array of MTJs on said first conductive layer and forming a planar third insulation layer on said second insulation layer and first conductive layer wherein said third insulation layer is coplanar with said MTJs;

(c) forming a second conductive layer which is a lower metal layer comprised of a plurality of parallel second lines having a first thickness and a first width on said MTJs and third insulation layer, said second lines are formed in and are coplanar with a dielectric layer;

(d) forming a fourth insulation layer on said second conductive layer and dielectric layer and forming openings over portions of said second lines that are not above said MTJs;

(e) forming a fifth insulation layer on said fourth insulation layer and second lines and forming a pattern comprised of a plurality of first trenches having sidewalls and bottoms on said fourth insulation layer and above said MTJs and a plurality of second trenches having sidewalls and bottoms on portions of said second lines that are not above said MTJs;

(f) depositing a conformal diffusion barrier layer on the sidewalls and bottoms of said first trenches and second trenches and depositing an upper metal layer on said diffusion barrier layer that fills said first and second trenches; and

(g) planarizing said diffusion barrier layer and upper metal layer to be coplanar with said fifth insulation layer thereby forming parallel third lines in said first trenches, and thicker regions of said second lines where a second trench is formed on said lower metal layer wherein a lower metal layer, an overlying diffusion barrier layer, and an upper metal layer on the diffusion barrier layer form a thicker region that has a second thickness greater than said first thickness.

12. The method of claim **11** wherein said sectioned first lines are bottom electrodes, said second lines are bit lines, and said third lines are word lines.

13. The method of claim **11** wherein said first thickness is about 0.02 to 0.3 microns and said first width is about 0.3 to 1.2 microns.

14. The method of claim **11** wherein an MTJ is formed at each location where a second line crosses over a sectioned first line.

15. The method of claim **11** wherein said openings are trenches and are formed over portions of said second lines where a second trench is formed in a subsequent step.

16. The method of claim **11** wherein said fourth insulation layer has a thickness between about 0.01 and 0.3 microns.

17. The method of claim **11** wherein forming said first trenches and second trenches is comprised of forming a photoresist pattern on said fifth insulation layer, selectively etching said fifth insulation layer, and stopping on said fourth insulation layer at the bottom of said first trenches and on said second lines at the bottom of said second trenches.

18. The method of claim **17** wherein said fifth insulation layer has a thickness between about 0.05 and 0.5 microns and has a different composition than the fourth insulation layer in order to provide sufficient etch selectivity during the formation of the first and second trenches.

19. The method of claim **18** wherein the fourth insulation layer is comprised of Al_2O_3, the fifth insulation layer is comprised of silicon oxide, and said selective etching involves a plasma etch with a fluorine containing gas.

20. The method of claim **11** wherein said first trenches have a length of about 0.2 to 0.8 microns.

21. The method of claim **11** wherein said second trenches have a length of about 0.5 to 1.5 microns.

22. The method of claim **11** wherein the fifth insulation layer has a width of about 0.1 to 0.2 microns between a first trench and a second trench.

23. The method of claim **11** wherein said lower metal layer is comprised of a diffusion barrier layer and a conductive layer on the diffusion barrier layer and said conductive layer is comprised of the same metal as in the upper metal layer.

24. The method of claim **11** wherein said second thickness is between about 0.08 and 1.1 microns.

25. The method of claim **11** wherein the upper metal layer has a width about equal to the first width of the lower metal layer.

26. The method of claim **11** wherein said sectioned first lines are comprised of Ta, Ru, W, Al, or Cu and said second lines are comprised of copper or gold.

27. An MRAM array, comprising:

(a) a first conductive layer comprised of a plurality of first conductive lines formed on a substrate;

(b) a second conductive layer comprised of a plurality of parallel second lines which are formed above said first conductive lines, said second lines have thinner and thicker portions; and

(c) a plurality of MTJs wherein an MTJ is formed at each location where a second line crosses over a first conductive line.

28. The MRAM array of claim **27** wherein the first conductive lines are bottom electrodes formed on a first insulation layer and within a second insulation layer that is on said first insulation layer.

29. The MRAM array of claim **28** wherein said MTJs are coplanar with a third insulation layer that is formed on said second insulation layer and first conductive lines.

30. The MRAM array of claim **27** wherein said second conductive layer is comprised of second lines which are bit lines.

31. The MRAM array of claim **30** wherein a thinner region of a bit line is formed above an MTJ and has a thickness of about 0.02 to 0.3 microns.

32. The MRAM array of claim **30** wherein a thicker region of a bit line is not formed above an MTJ and has a thickness of about 0.08 to 1.1 microns.

33. The MRAM array of claim **30** wherein a thinner region of a bit line is a lower metal layer comprised of a first diffusion barrier layer or adhesion layer and a conductive layer which is copper or gold formed on the first diffusion barrier layer or adhesion layer.

34. The MRAM array of claim **33** wherein a thicker region of a bit line is comprised of a portion of the lower metal layer, an overlying second diffusion barrier layer, and an upper metal layer on the second diffusion barrier layer.

35. The MRAM array of claim **34** wherein said first and second diffusion barrier layers are comprised of a composite layer which is Ta/TaN or Ti/TiN and said upper metal layer has the same composition as the conductive layer in the lower metal layer.

36. The MRAM array of claim **29** further comprised of a fourth insulation layer formed on the third insulation layer, a fifth insulation layer on the fourth insulation layer, and an array of parallel word lines formed above said MTJs in said fifth insulation layer wherein said word lines are perpendicular to said bit lines.

37. An MRAM array, comprising:

(a) a first conductive layer comprised of a plurality of first conductive lines formed in a second insulation layer on a substrate that has an upper first insulation layer;

(b) an array of MTJs formed on said first conductive layer and within a third insulation layer that is coplanar with said MTJs;

(c) a second conductive layer that is comprised of a plurality of parallel second lines on said MTJs and third insulation layer, said second lines have thinner portions comprised of a lower metal layer formed above said MTJs and thicker portions comprised of a second trench on said lower metal layer wherein a second trench has a conformal diffusion layer formed therein and a planar upper metal layer formed on the diffusion barrier layer that fills said second trench;

(d) a dielectric layer formed between said second lines and coplanar with said second lines;

(e) a fourth insulation layer formed on said dielectric layer and parallel second lines and a fifth insulation layer which is coplanar with said upper metal layer and is formed on said fourth insulation layer; and

(f) a plurality of first trenches which are an array of parallel third lines formed within said fifth insulation layer above said MTJs wherein each first trench has sidewalls and a bottom on said fourth insulation layer, a conformal diffusion barrier layer formed on said sidewalls and bottom, and an upper metal layer formed on said diffusion barrier layer that fills said first trench and is coplanar with said fifth insulation layer.

38. The MRAM array of claim **37** wherein said first conductive lines are bottom electrodes, said second lines are bit lines, and said third lines are word lines.

39. The MRAM array of claim **37** wherein said second lines have a width of about 0.3 to 1.2 microns.

40. The MRAM array of claim **37** wherein an MTJ is formed at each location where a second line crosses over a first conductive line.

41. The MRAM array of claim **37** wherein said fourth insulation layer has a thickness between about 0.01 and 0.3 microns.

42. The MRAM array of claim **37** wherein said fifth insulation layer has a thickness between about 0.05 and 0.5 microns and has a different composition than the fourth insulation layer.

43. The MRAM array of claim **37** wherein said thinner portions of a second line have a thickness of about 0.02 to 0.3 microns.

44. The MRAM array of claim **37** wherein a thicker portion of a second line has a thickness between about 0.08 and 1.1 microns.

45. The MRAM array of claim **37** wherein said second trenches have a length of about 0.5 to 1.5 microns.

46. The MRAM array of claim **37** wherein said first trenches have a length of about 0.2 to 0.8 microns.

47. The MRAM array of claim **37** wherein the distance between a first trench and a second trench is about 0.1 to 0.2 microns.

48. The MRAM array of claim **37** wherein said lower metal layer is comprised of a diffusion barrier layer and a conductive layer formed thereon and the conductive layer is comprised of the same metal as in the upper metal layer.

49. The MRAM array of claim **37** wherein a first conductive line is comprised of Ta, Ru, W, Al, or Cu and said second lines and third lines are comprised of copper or gold.